

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

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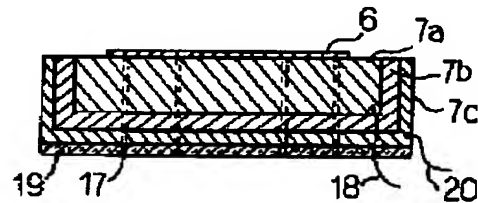
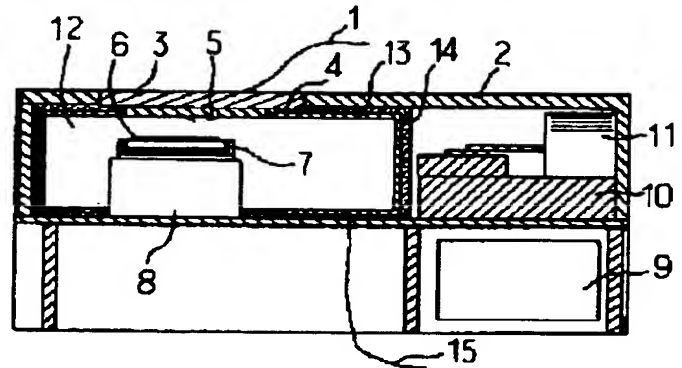
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APPLICANT : MITSUBISHI ELECTRIC CORP;

INVENTOR : YAMADA TSUYOSHI;

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TITLE : SEMICONDUCTOR TEST DEVICE



**ABSTRACT :** PROBLEM TO BE SOLVED: To prevent false judgment and enable good wafer test results in a test of a semiconductor integrated circuit in wafer state by constituting a chuck top of a shield part, an insulation layer and a bias electrode part whereon a semiconductor integrated circuit is mounted and covering a shield wall with an insulation layer.

**SOLUTION:** The whole test execution area 12 of a semiconductor integrated circuit 6 in wafer state is made a shield chamber. A shield wall 13 for shielding a circumference of a chuck top 7 from external noises is provided. The chuck top 7 includes a bias electrode part 7a for fixing electric potential of a rear of the semiconductor integrated circuit 6, a shield part 7c and an insulation layer 7b for insulating the shield part 7c electrically. The inner wall of the whole test execution area 12 is covered with the shield wall 13 through an insulation layer 14 electrically insulating from a frame part 2 of a wafer prober, and is connected by a GND connection line 15. Thereby, noises can be prevented from arriving on a semiconductor integrated circuit 6 in wafer state.

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